

specification with informal examiner's amendments

## BACKGROUND

### 1. Field of the Invention

This invention relates to data communications in a computer system, and more specifically, to a memory translator hub designed to provide a memory bus from a memory channel.

### 2. Background Information

Computer systems rely heavily upon Dynamic Random Access Memories ("DRAMs") to implement system memories due to their simplicity, affordability and memory density. However, it is increasingly difficult to design memory systems that satisfy the size and performance requirements for modern computer systems using DRAMs connected by conventional bus architectures. To overcome these limitations, a memory subsystem can be constructed using a memory channel architecture. Intelligent memory devices are connected by a narrow, high-speed bus, termed a channel. Packets of information are transmitted on the memory channel to communicate between the memory controller and the memory devices. Direct Rambus™ architecture using Rambus® channels is an example of a memory subsystem using a memory channel architecture.

As a new technology, the cost of components, such as Rambus DRAM (RDRAM™), for memory channel subsystems is high and supplies are uncertain. Memory channel devices require a completely different memory interface from conventional memory devices. Memory channel devices are not compatible with